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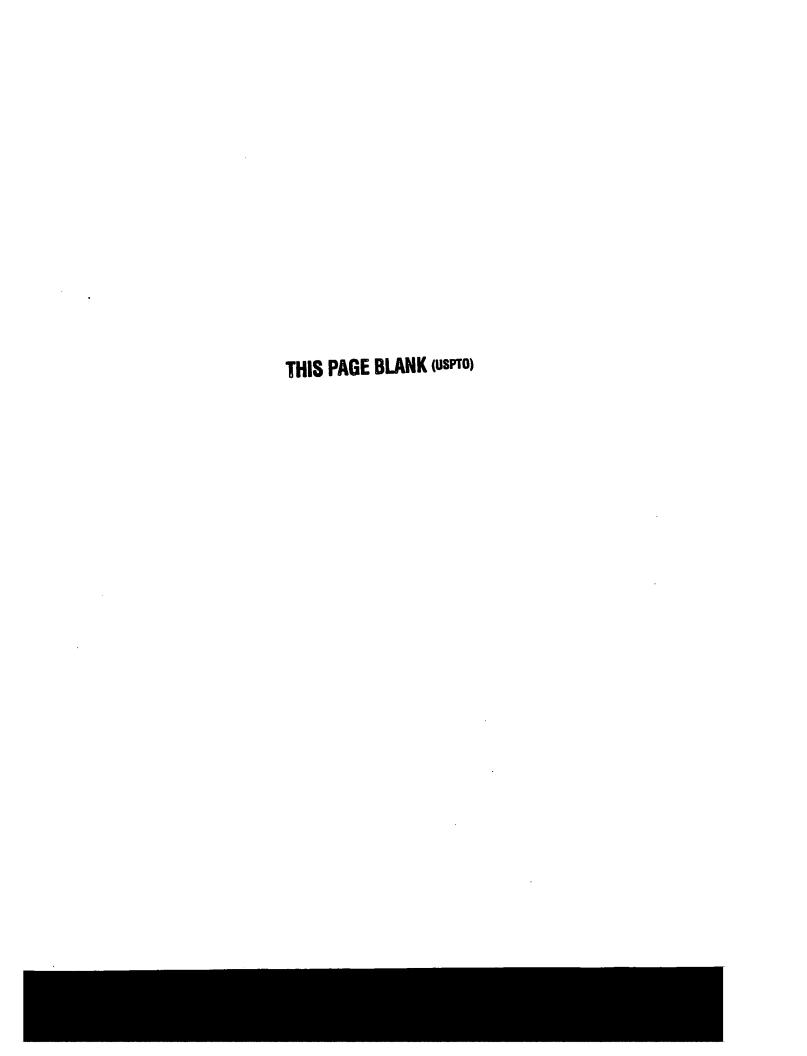
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UK Patent Application (19) GB (11) 2 077 036

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5000 - 0 60 E (21) Application No 8114853 (22) Date of filing 14 May 1981 (30) Priority data (31) 149968 _(32)_15 May 1980 (US), 5A4:5E2 RL GB 1469085 GB 1277254 GB T245710 ----(58) Field of search "H1K""" (7.1) Applicant · CTS-Corporation__1 905 North West Boulevard Eikhart Indiana 46514

(54) Multi-layer ceramic package for semiconductor chip ...

(57) In a multi-layer ceramic package wherein a plurality of ceramic laminates each has a conductive (33) United States of America internal cavity of the package within Application published internal cavity of the package within a Dec 1981 which is bonded a chip or a plural-38(61) INT CL3 HOLL 23/12[364 ity of ohips interconnected to form a chip array, the chip or chip array d((52)\Domestic classification() (16) is connected through short າເຄົ້າ HIK 4C11 4C1U 5Aາເກັ່ງ kwire boinds (42) at varying laminate A 4 349: 1 levels each having metalized con-6.2 (56) Documents cited : 359 3 ductive patterns thereon, and the GB 2004127A

CONTROL TO THE PROPERTY OF THE PR nected either by tunnel openings (32) filled with metalized material, or by edge formed metalizations ---- (34) so that the conductive patterns ાકુ 🛴 ૧૯૬૩ ultimately connect to a ဥnumber of pads at the undersurface of the ceramic package when mounted on

to a metalized board. There is achieved a high component density, but because the connecting wire leads"are" "staggered" or connected at alternating points at package levels, it is possible to maintain a 10 mil spacing and 10 mil size of the wire bond lands.

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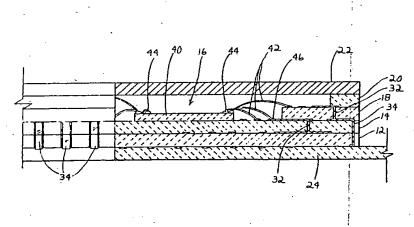


FIG. 3

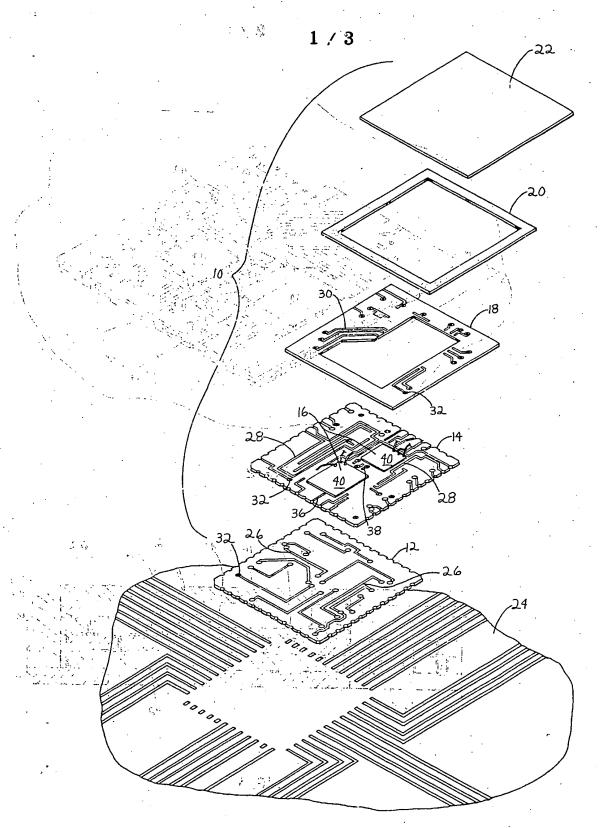
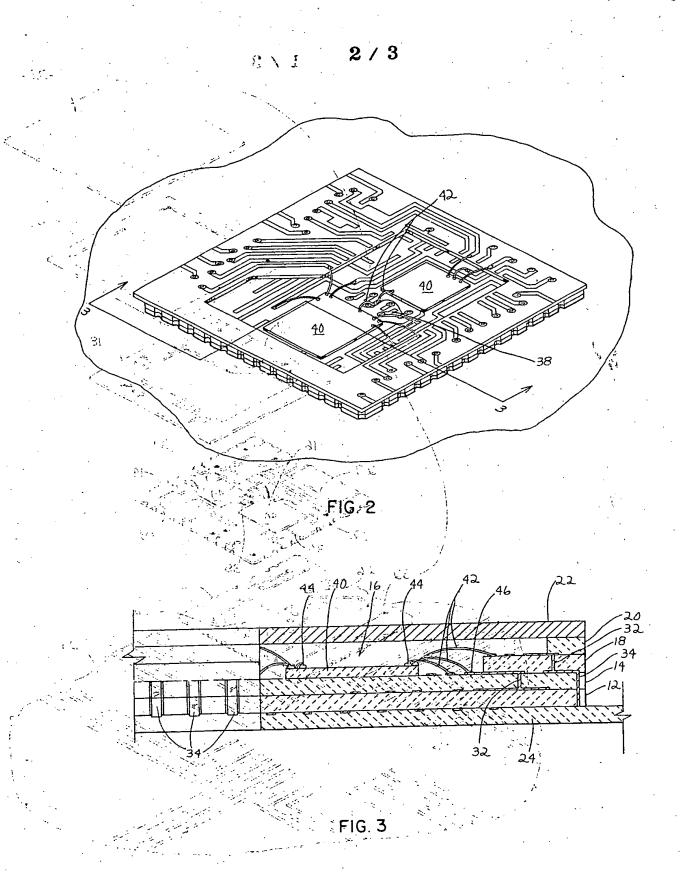


FIG. I



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SPECIFICATION

Multi-layer ceramic package 🧠 🦠

5 In the packaging of interconnected chip or chip arrays, wire bondings from the chip or chip array, particularly where there is a high component density, or where bonding pads on chips are closely spaced, are excessively

10 crowded, so that there is a real danger that the wire bonds will come into too close proximity with each other and present a serious difficulty in maintaining required spacing for the wires and the bonding lands. This is

15 because the conductive patterns converge upon the chips from the printed metalized patterns provided on the single ceramic laminate. The result is overcrowding of the wire conductors or bondings. However, the trend

20 in multiple circuit chip structures is toward
even greater component density, and the conductive patterns on the ceramic package must
nevertheless be wire bonded to the chips of
the array.

Thus, the technology trend, headed as it is toward even greater component density, presents serious and thus far unsolved problems of how to achieve the necessary pin outs, from LSt arrays through wire bondings to the

metalized conductive patterns, while still maintaining an industry imposed standard of it is an object of the invention to provide a solution to this problem.

35 In accordance with one aspect of the present invention, there is provided a high component density, multi-layer chip carrier in which wire bonds are connected to a single chip or to chips interconnected in a chip

40 array, with the wire bondings then disposed for pin-outs at alternately different layers in the ceramic package, thus achieving greater clearance for the respective wire bonds and wire bonding lands.

The present invention makes it possible to increase the density of an interconnected LSI chip array while at the same time providing the necessary pin outputs for wire bondings leading to such array and while maintaining the requisite 10 mil spacing and 10 mil width

of metalized wire bonding lands.
In accordance with a further feature of the invention, there is provided an interconnected chip array disposed within a cavity of a multi-

55 layer ceramic package, in which the wire bonds are successively secured between the chip array at one end and to different levels of a multi-layer ceramic package at the other end. The respective levels of the ceramic

opackage are individually metalized for a particular conductive pattern, and the patterns are connected through either or both of metalized connections in the form of "tunneled through" openings from one layer to the other edge metalizations so that the respective con-

ductive patterns are connected, leading ultimately to a series of pads at the undersurface of the ceramic package.

Generally, therefore, the present invention 70 provides a multi-layer ceramic package having various level laminates each with a particular conductive pattern, the patterns on the respective layers being connected by either tuningled through or edge metalization bonding,

75 or both. Various pin outs from a central disposed interconnected chip array, disposed within a cavity are connected through wire bonds with said patterns while maintaining an appropriate spacing one relative to the other.

80 According to another aspect of the present invention, there is provided a method for producing a high component density multilayer chip carrier, comprising the steps of forming a first chip carrier, layer adapted to 85 receive at least one chip thereon, and at least

one additional layer, forming pin-out conductive connections with said chip, forming metalized conductor paths on said respective layers, and forming wire connections from said

90 chip alternating between staggered paths respectively formed on the differing levels of said layers.

Further features of the present invention will become apparent from a consideration of 95 the following description which proceeds with reference to the accompanying drawings in which selected example embodiments are illustrated by way of example and not by way of limitation.

100 In the accompanying drawings:

Figure 1 is an isometric exploded view illustrating a multi-layer ceramic package, with a printed circuit board at the lower portion and a combination ring and cover at the 105 upper portion which seals an internal cavity in

105 upper portion which seals an internal cavity in the ceramic package for receiving a chip array:

Figure 2 is an isometric detail view of a multi-layer ceramic package with the ring and 110 cover removed;

Figure 3 is a cross sectional view taken on line 3-3 of Fig. 2 showing the metalized edges, tunnels, and wire bond-pattern connections between the chip array and the various 115 levels of the multi-layer ceramic package;

Figure 4 is the undersurface of the base layer of the ceramic package to be mounted to the metalized board;

Figure 4A is the upper surface of the base 120 layer of the ceramic package and is the opposite face to that of Fig. 4; and

Figure 5 is an enlarged detail view of the ball bond and wedge leads of the wire between the chip array at one wire end and a 125 respective layer of the ceramic package at the other wire end.

Referring to Fig. 1, a multi-layer ceramic package designated generally by reference numeral 10 includes multi-layers of ceramic sub-130 strate including a base layer 12, intermediate

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layer 14 on which is mounted an interconnected chip array 16, an upper frame layer multi-layer ceramic package as a whole is mounted on a metalized board 24.

The base layer 12, intermediate layer 14, and frame layer 18 each has a printed conductive pattern illustrated by reference numeral 26 in the base layer 12, by reference numeral 28 in the intermediate layer, and by reference numeral 30 for the frame layer 18. The particular pattern of these conductive metalization paths is not a part of the present invention. However, it is contemplated that, 15" prior to assembly, the "green" or unfused ceramic substrates have formed thereon the the different conductive patterns which are then matched together and electrically connected through connections leading ultimately to pads 33 on 20 the undersurface 31 (Fig. 4) of the base layer 40 3.00 %12 for the metalized board 242 accounts

tions depliffice conductive patterns are communicated entanth one layer with the next, in one instance BC 16 Dithrougher tunnels" 32 (Fig. 3) which are in 25 the form of vertical through openings filled ductive patterns of one layer to the next. In a supportunnel and edge metalizations are formed his conductive patterns of the respective laminates are connected 30 through edge metalizations 34 (Fig. 3).

The interconnected chip array 16 consists of component LSI chips which are connected the centrally disposed array, are surmounted is together. The chips are connected by metalization printed circuits constructed on the con-35 fronting surface of intermediate layer 14, and indicated by reference numeral 36: 001

host a from a chip first outwardly to the periphery of 40 the package and then back to another chip, "there can be chip to-chip wire bonding i through lands 38 disposed between and sepdesignated generally by reference numeral 42. There is thus provided the interconnections necessary to form a high density interno bed not els in the multi-layer ceramic package. connected chip array which has pin out connections to the conductive patterns at the respective laminations of the multi-layer ce-50 ramic package: 103 - 3 ton one bush 32653

With the high component density dei scribed, it is difficult to maintain the 10 mil of box architecture and componentry. spacing which is required for conductive patterns. This is achieved, in accordance with a feature of the present invention, in the man-60 other end through a wedge bond 46 to a conductive pattern on one or the other of the intermediate layer 14 or frame layer 18. In spite of the high density of LSI chip components and wire bonds, the 10 mil spacing of 65 the conductive patterns is maintained by alter-. 3"1

nating between layers 14 and 18: to the Obviously, there can be more than two 18, a ring layer 20, and a cover layer 22. The attracting layers; three, four or even more tations layers for alternate wire bonding are contem-11 vi70, plated. However, the basic concept, generally, is that by coupling the wire bonds between the centrally disposed high density chip array, and alternately differing levels of the metalized layers, it is possible to increase the 75 number of wire bonds and thus achieve the desired centrally disposed component, density while in no way compromising the necessary 10 mil spacing for the conductive patterns. . With regard to manufacture, the wire bonds 80 between the central array and the conductive patterns at the various levels make appropriate connections from layer-to-layer as de-.... scribed, either through tunnels 32 or edge metalizations 34 (Figs. 3 and 4a) all of which ultimately lead to the base layer 12 and underlying pads 33 which are then bonded to appropriate locations on the underlying metalized board 24. The laminants may typically consist of aluminum silicate or other inert 90 substrate materials, which, as stated previwith metalization, and which connect the con- up and ously, are green at the time the metalizations,

The layers having a conductive pattern, the 95 ring 20, and the chip array, once the chip and wire bondings made with with cover layer 22. The package as a whole

is next fired (sealed) and the final product 100 mounted on to the metalized board 24.

The chip array is mounted on the intermedi-Between the chips, and to obviate the ne-option, that layer 14, and the chips 40 of the array Cessity for the wire bondings to be connected equity are communicated chip-to-chip through lands 38 on the upper face of the intermediate layer 105 14, and other layers as required.

man interpretations as required. arating the chips 40. These wire bonds are entropy terns, made by bonding the ends of the wire bonds so that adjacent wire bonds are con-1,10 nected from the chip array to alternating lev-

> The package as a whole is next mounted on the metalized board 24 so that the page 33 at If you hit the exterior surface of the package are ating 1.15 mounted on various terminals of the metalized 1916 gra, board having a predetermined printed circuit

...It should be understood that any required inconductive pattern can be screened on to the 120 surface of the respective layers of the multiner illustrated in Figs. 2 and 3. As shown in the layer ceramic package, and the conductive the chip array connected at one end through a second pattern per se, for example as illustrated, ball bond 44 (Fig. 5) to a chip 40 and at the in a seedoes not form a part of the present invention.

It should be further emphasised that the 10 ritionil spacing is achievable in the present invention by reason of connecting first one wire from the chip array to a first level and then an alternating the wire bonds to a second level, a 130 third level, a fourth level, etc., thereby provid-

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11. 14.

ing the means for maintaining aid mil of conductive patterns spacing in spite of the increased component density and the central converging of such wires. Quite obviously, if 5 the 10 mil spacing is not maintained as an industry standard, it is equally possible to obtain an even higher component density with either an agreed upon less than 10 mil spacing and/or less than 10 mil bonding lands.

In all events, the present invention provides the possibility of maximum component density while maintaining a 10 mil spacing, but is a 1 to 7. A multi-layer ceramic package, comprisequally applicable to whatever component density is desired, while achieving an inher-15 ently greater density for the respective wire bonds...

to dw lottly Although the present invention has been illustrated and described in connection with a single example embodiment, it will be under and bob single example embourners, will be attended to be a specific and the invention and is by no means restrictive thereof. For example, instead of three ceramic layers of ing, multi-layering, and various arrangements for the printed circuit network as well as the decertical connections from the chip to said architecture of interconnected chip array. All of these changes are contemplated as part of 18 A multi-layer ceramic package in account of these changes are contemplated as part of 18 A multi-layer ceramic package in account of the present invention and it is intended that 18 and 95 dance with claim 7, wherein said predetersuch variations shall be included within the become mined spacing is 10 mil. scope of the invention as defined by the Scope of the process and was at the following claims. The content of the between the following the content of t

layer adapted to receive at least one chip 40 thereon, and at least one additional layer, forming pin-out conductive connections with the but tramic laminants, whereby composite conductive to the state of the sta on said respective layers, and forming wire connections from said chip alternating be-

the different levels of said layers.

The method in accordance with claim

including the steps of forming said multilayers of individually compacted ceramic particeramic layers to sinter the particles and to

or claim 2, including the step of olspooning to disposing the country of cluding means forming an internal cavity of the country of the count outer face of said multi-layer carrier and adapted to serve as outlets on a metalized are a far inter-connecting the chip. noine value Olimpht Live

(LAVII. 160 or claim 2 or claim 3, including the steps of 1000 wherein said laminants are formed as comor claim 2 of claim 5, mode on the layer 7.11 adapted for receiving chips and effecting short; and quently fired to develop bonded inter-layer wire bonding between respective chips

15. The method in accordance with any of claims 1 to 4, including the step of sealing an interior cavity of said carrier which receives said chip and wherein said chip is mounted.

di bira

- 6....The method in accordance with any of 70 claims 1 to 5, including the step of disposing said wire connections between the chip and the metalized paths of said layers in alternating multi-level connections between said chip.

75 and layers to not less than two alternating av adayers of said multi-layer chip carrier.

北京 ingla plurality of spaced apart laminants inbase cludingian intermediate level laminant

it 80 adapted to receive a chip array, at least one debachipidisposed on said intermediate level lamidges at nanta conductive patterns on respective ones Selected ones of said laminants, selected ones of said conescoudive patterns having wire bonds, metalized 85 conductive means interconnecting the conduchade Your tive patterns on the respective multi-layered see laminants, and wire connections maintaining the multi-layer ceramic package, it is possible the mot less than a predetermined spacing of said wire bonds respectively by extending between 25, achieve the desired combination of wire space >90 said chip at one end and to alternating levels wire bonds respectively by extending between terrof laminants at the other end to provide resconductive patterns, we suggest a

1, 8) FA multi-layer ceramic package in accor-

Hintern (d.) 900cThe, multi-layer, ceramic, package in aces are cordance with claim; 7 or claim, 8 wherein the br . 44 sconductive means comprises metalized-filled 100 openings, forming conductive, paths between TOU openings forming conductive paths between the conductive patterns on respective sides of nent density multi-layer chip carrier, comprises a selective ones of the laminants forming the ing the steps of forming a first chip carrier to visit to ceramic package, and edge-formed metalized 11 do a conductive paths interconnecting the conduc-105 tive patterns on other of the multi-layer ce-

said chip, forming metalized conductor paths and active patterns of said aminants are connected farminitogether, and to, said, chiper a some அகரும் வர் 1.0 ு ் The multi-layer ceramic package in

45 tween staggered paths respectively formed on 91.1 1.0 accordance with any of claims 7 to 9, includio. 100 ling means forming lands at the level of the ed 1 ceramic package wherein a chip array is disand short wire bond connections to the land providing a conductor network between 1:165 the chips of the chip array, said multi-layer in to ceramic package being adapted for high com-

bond the respective layers together.

bond the respective layers together.

The multi-layer ceramic package in or claim 2, including the step of disposing a use of accordance with any of claims 7 to 10, inlayers, and providing a plurality of pads at the and a said package, the intermediate level laminant ரிறுகள் Lincludes internal cavity lands for electrically

4. The method in accordance with claim 1 125 accordance with any of claims 7 to 11, pacted ceramic particle layers, and subsemalls vill connections between confronting surfaces of 130 the respective ceramic laminants.

65 through said lands.

The multi-layer ceramic package in 13. Caccordance with any of claims 7 to 12, including a high component density chip array,

an internal cavity for receiving said high component density chip array, means forming an அந்த நடி interconnected relation of said chips and wire bonds from said interconnected chip array to alternating levels of conductive patterns on the respective multi-level ceramic laminants to

10 form a multi-layer ceramic framing for said multi-layer ceramic package.

14. A method of producing a multi-layer chip carrier substantially as hereinbefore described with reference to the accompanying 15 drawings. Sale and the North Advantage

15. A multi-layer ceramic package substantially as hereinbefore described with reference to the accompanying drawings.

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